Applicants	Linn et al.	**COMMUNICATION REGARDING CERTIFICATE OF CORRECTION**
Patent No.	6,909,146	
Issue Date	6/21/2005	
Serial No.	09/316,580	
Attorney Docket No.	125.064US05	
Title: BONDED WAFER WITH METAL SILICIDATION		

ATTN: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Applicants hereby request issuance of a Certificate of Correction in U.S. Letters Patent No. 6,909,146 as specified on the attached Certificate (Form PTO/SB/44). Please find enclosed documentation supporting errors identified in the above noted patent, referred to herein as Exhibits A and B.

With respect to the error identified in claim 3 of the issued patent, Exhibit A is a copy of pages 1 to 5 of an Amendment under 37 CFR 1.312 (including claim 3 as allowed) and a signed Certificate of Transmission indicating filing of the Amendment with the U.S. Patent & Trademark Office on May 20, 2004. Exhibit B is a copy of Cols. 9 and 10 of the issued patent. The identified error constitutes a typographical error and as such, does not introduce new matter.

Applicants believe this correction as specified is necessary due to an Office error and do not believe that any fee is due for requesting a Certificate of Correction for this patent. However, if deemed necessary, the Office is authorized to charge any additional fees found due to Deposit Account No. 502432. Please contact the undersigned if you have any questions.

Respectfully submitted,

Date: December 14, 2007

/David D. Freitag/

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Enclosures

Applicant	Jack H. Linn et al.	**AMENDMENT UNDER 37 C.F.R. §1.312**
Serial No.	09/316,580	
Filing Date	May 21, 1999	
Group Art Unit	2811	
Examiner Name	Steven Loke	
Confirmation No.	7991	
Attorney Docket No.	125.064US05	
Title: BONDED WAFER WITH METAL SILICIDATION		

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Please amend the above-identified application as follows:

Amendments to the Specification begin on page 2 of this paper.

The Claims begin on page 5 of this paper.

Remarks begin on page 8 of this paper.

Amendments to the Specification:

Please amend the **Summary of the Invention** as follows:

Summary of the Invention

The present invention is directed to a silicon-on-insulator integrated circuit that comprises a handle die, a substantially continuous and unbroken silicide layer over the handle die, and a substantially continuous and unbroken first dielectric layer overlying one side of the silicide layer. A device silicon layer having an upper surface overlies the first dielectric layer, and a second dielectric layer on the handle die underlies the opposite side of the silicide layer. Interconnected transistors are disposed in and at the upper surface of the device silicon layer.

Also in accordance with the present invention is a silicon-on-insulator integrated circuit that includes a handle die and a first dielectric layer formed on the handle die. A substantially continuous and unbroken silicide layer is formed on the first dielectric layer; the silicide layer has a controlled resistance and provides a diffusion barrier to impurities. A substantially continuous and unbroken second dielectric layer is disposed between the silicide layer and a device silicon layer, and trenches extend through the device silicon layer and silicon layer and separate the device silicon layer into islands, each having an underlying continuous silicide area. Interconnected transistors are disposed in and at an upper surface of the device silicon layer.

The present invention is further directed to a bonded wafer integrated circuit that comprises a handle die and a homogeneous silicide layer bonded to the handle die. A device layer is bonded to the silicide layer, and interconnected transistors are disposed in and at a surface of device layer. ~~The silicide layer comprises bonding material that differs from material in the portion of the handle die adjacent the silicide layer and also differs from material in the portion of the device layer adjacent the silicide layer.~~

The present invention provides silicon-on-insulator bonded wafer processing with the features of (1) relatively low temperature bonding by the use of low temperature, about 500-800° C metal silicidation reactions for bonding; (2) better stress compensation

by providing materials in the bonding zone that will produce silicides with coefficients of thermal expansion closely matched to those of the substrate wafers and buried dielectric layers, thereby reducing warpage; (3) limiting contaminant migration by means of a bonding zone that provides a barrier to diffusion of mobile contaminants; (4) simultaneously producing a buried doped layer in the silicon during the bonding process; (5) a conductive, dielectrically-isolated layer at the bonding zone; and (6) a thermally conductive layer at the bonding zone.

Please amend the **Abstract** as follows:

A silicon-on-insulator integrated circuit comprises a handle die, a substantially continuous and unbroken silicide layer over the handle die, and a substantially continuous and unbroken first dielectric layer overlying one side of the silicide layer. A device silicon layer having an upper surface overlies the first dielectric layer, and a second dielectric layer on the handle die underlies the opposite side of the silicide layer. Interconnected transistors are disposed in and at the upper surface of the device silicon layer. A silicon-on insulator integrated circuit includes a handle die and a first dielectric layer formed on the handle die. A substantially continuous and unbroken silicide layer is formed on the first dielectric layer; the silicide layer has a controlled resistance and provides a diffusion barrier to impurities. A substantially continuous and unbroken second dielectric layer is disposed between the silicide layer and a device silicon layer, and trenches extend through the device silicon layer and silicide layer and separate the device silicon layer into islands, each having an underlying continuous silicide area. Interconnected transistors are disposed in and at an upper surface of the device silicon layer. A bonded wafer integrated circuit comprised a handle die and a homogeneous silicide layer bonded to the handle die. A device layer is bonded to the silicide layer, and interconnected transistors are disposed in and at a surface of device layer. ~~The silicide layer comprises bonding material that differs from material in the portion of the handle~~

~~die adjacent the silicide layer and also differs from material in the portion of the device layer adjacent the silicide layer.~~

Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

Listing of claims:

Claims 1-3 and 7-9

1. A silicon-on-insulator integrated circuit, comprising:

(a) a handle die;

(b) a substantially continuous silicide layer over said handle die,

(c) a substantially continuous first dielectric layer overlying one side of said silicide layer;

(d) a device silicon layer overlying said first dielectric layer, said device silicon layer having an upper surface;

(e) a second dielectric layer on said handle die underlying the opposite side of said silicide layer; and

(f) interconnected transistors in and at the upper surface of said device silicon layer.

2. The integrated circuit of claim 1 wherein said silicide layer comprises a diffusion barrier to impurities.

3. The integrated circuit of claim1 further comprising:

(g) trenches extending through said device silicon layer and separating said device silicon layer into islands.

4-6. (Cancelled)

EXHIBIT A

Applicant	Li[illegible]t al.
Serial No.	09/316,580
Filing Date	May 21, 1999
Group Art Unit	2811
Examiner Name	Steven Loke
Facsimile No.	703-872-9306
Attorney Docket No.	125.064US05

FACSIMILE TRANSMITTAL FORM

Title: BONDED WAFER WITH METAL SILICIDATION

TOTAL PAGES: 8 pgs. (including cover sheet)
TO CENTRAL FAX – (703) 872-9306
Attention: Examiner Steven Loke, Art Unit 2811

US Patent and Trademark Office
2001 South Clark Place
Customer Window
Crystal Plaza Two, Lobby, Room 1B03
Arlington, VA 22202

Enclosures

The following documents are enclosed:

X Amendment Under 37 C.F.R. §1.312 (7 pgs.).

Submitted By

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Certificate of Transmission

I certify that this paper, and the above-identified documents, are being transmitted by facsimile to, Examiner Steven Loke, Group Art Unit 2811 (Facsimile No. 703-872-9306) of the United States Patent and Trademark Office on May 20, 2004.

Name	Elizabeth A. Bauer	Signature	

(d) a device silicon layer overlying said first dielectric layer, said device silicon layer having an upper surface;

(e) a second dielectric layer on said handle die underlying the opposite side of said silicide layer; and

(f) interconnected transistors in and at the upper surface of said device silicon layer.

2. The integrated circuit of claim **1** wherein said silicide layer comprises a diffusion barrier to impurities.

3. The integrated circuit of claim **1** further comprising:

(g) trenches extending through said device silicon layer and separating said dice silicon layer into islands.

4. A silicon-on insulator integrated circuit comprising:

(a) a handle die;

(b) a first dielectric layer formed on said handle die

(c) a substantially continuous silicide layer formed on said first dielectric layer, said silicide layer having a controlled resistance and providing a diffusion barrier to impurities;

(d) a substantially continuous second dielectric layer disposed between said silicide layer and a device silicon layer;

(e) trenches extending through said device silicon layer and silicide layer and separating said device silicon layer into islands each with an underlying continuous silicide area; and

(f) interconnected transistors in and at an upper surface of said device silicon layer.

5. The integrated circuit of claim **4** further comprising:

(g) trenches extending through at least one of said islands to said underlying silicide area, said trenches having dielectric sidewalls and containing conductive material in contact with said silicide area.

6. The integrated circuit of claim **5** wherein said islands have a thickness no greater than about 2 μm, and said conductive material is tungsten.

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